

Case Study: Memory pooling Test Chip

Parameter	Data
Scope Summary	Complete responsibility from Synthesis to Final GDS with all quality signoff checks for Testchip
Engagement Model	Turnkey
Technology	Technology - 7nm Size : 9x12 mm Gate count: 70 mn 0.75V(nominal), 100C Routing: 14 layers (for block level) + GM0 and GM1 for the top
Targets & Signoff Conditions	• Frequency – 1.6GHz, 400MHz • 1 Functional Mode • 2 corners
Design Flow	• Native design flow • Chip level design planning and partitioning • System bus partitioning and placement • Repeater (source sync data transfer) planning and automated APR till routing • Signoff (STA, PV, FEV, VCLP, RV) closure for 40+ partitions and SoC level]
Team / Duration	40 (Skills: Synthesis/SD/STA/LV/RV/Signoff) / 12 months
Challenges	• Design planning for over all chip and pin placement • System bus partitioning and placement (9 partition → 3 partition -> 7 partitions) • Repeater (source sync) data transfer across chip and so re-structuring RTL and DP • Automated APR for all 16 repeaters and then timing closure • Timing closure with DDR and other High-speed IP • PV closure -boundary level PV violations because of pin placement • Schedule (because of multiple RTL release)

Case Study: High Bandwidth Memory IO Hardening with TSV

Parameter	Data
Scope Summary	Complete responsibility from Synthesis to Final GDS with all quality signoff checks
Engagement Model	OCB Model
Technology	Technology : 10nm Size: 1.5 x 6.1 mm 0.85V(nominal), 100C Routing: 14 layers (for block level) + GM0 and GM1 for the top
Targets & Signoff Conditions	• Frequency – 1.6GHz • 1 Functional Mode • 16 corners
Design Flow	RTL Modification and release through FEBE Functional Verification and GLS Shipment and contour flow RTL -> GDSII (block level implementation), Top level Integration, Bump Routing , (Synthesis, Floorplan, Placement, CTS, Route, STA, LV, RV, Caliber, FEV, VCLP, PTPX, crossfire) Database release
Team / Duration	16 (Skills: Synthesis/SD/STA/LV/RV/Signoff 10nm (1274.11) node) / 12 months
Challenges	• Clock tree building • Floor planning & placement (TSV) and TSV/PSB requirement (resulted in RTL changes) • Custom Routes • DCAP insertion • RV checks with TSV implementation • LV closure (V14 density closure)

Case Study: 10nm Full Chip Quad Core SoC

Parameter	Data
Scope Summary	Turnkey Implementation of Full Chip SoC Synthesis, DFT and APR of full chip SoC
Engagement Model	Turnkey
Technology	Technology - 10nm Size: 9 x 16 mm Gate count: 100 mn 0.75V (nominal), Temp -> 125C & -40C Total Routing Layers - 14 Top Metal Layer is used as RDL layer
Targets & Signoff Conditions	- Core Frequency, 400MHz - SS Frequency – 1.0 GHz - Functional Mode + Test mode (Scan Shift and Scan Cap Mode) 12 Timing corners
Design Flow	- Synthesis, DFT and APR and sign off partitions and SoC 100+ Partitions, Subsystems together - Integration of partitions and subsystems at SoC level - Best and well experienced managers and leads deployed - Dedicated architect to guide team - Detailed plan and schedule charted out (70 overall milestones defined, ~1000 tasks) - Early ramp up of teams to avoid delays - Close co-ordination between teams for effective collaboration - Close tracking of the progress and intermediate milestones
Team / Duration	120 (40+80) Skills: Synthesis/DFT/SD/STA/Physical Verification/Signoff 10nm / 15 months
Challenges	- Large team of Physical Implementation team, Effective co-ordination - Multi site, execution - Partitions were congested, timing critical 1.0GHz max frequency

